REMARKS

Claims 1, 2, 4-8 and 15-18 are pending.

In section 3 of the Office Action, Claims 1, 2, 4 and 5 are rejected under 35 USC § 102(e) as being anticipated by US patent publication No. 2002/0175846 (hereinafter referred to as "the Sakimura application"). Applicants are traversing this rejection.

The application contains two independent claims, namely Claims 1 and 4. Below, Applicants explain that the Sakimura application does not disclose all of the elements of Claims 1 and 4.

According to page 7, paragraph [0100] to page 8, paragraph [0101], the Sakimura application relates to a multi-bit ΔΣ A/D converter that comprises a first analog adder 1a coupled to a first analog integrator 2a, the first analog integrator 2a being coupled to a first analog multiplier 9a. The first analog multiplier 9a is coupled to a second analog adder 1b, the second analog adder 1b being coupled to a second analog integrator 2b. The second analog integrator 2b is coupled to a second analog multiplier 9b, an n-bit quantizer 4 being coupled to the second analog integrator 2b and a most significant bit extractor 5. The most significant bit extractor 5 is coupled to a third digital adder 10c via a so-called "digital processing port" 20 on a first branch and a pair of serially coupled digital differentiators 12a, 12b on a second branch. The most significant bit extractor 5 and the digital processing port 20 are coupled to the first and second analog adders 1a, 1b via a first delay element 8a and a one-bit D/A converter 6 on a feedback path.

The above described circuit configuration of the Sakimura application addresses quantization noise leakage in the analog integrators 2a, 2b due to non-linearities of the D/A converter 6.

Claim 1 recites a continuous time sigma delta converter that comprises conversion means having known non-ideal characteristics. The converter of Claim 1 also comprises a compensation circuit having error modeling components arranged to model substantially the non-ideal characteristics of the conversion means. A summation means is also coupled to combine a compensation signal generated by the compensation circuit and an output signal of the conversion means in order to provide a compensated output signal.

The Sakimura application does not teach "a continuous time sigma delta converter" as recited in Claim 1. The Sakimura application discloses, for example in relation to FIG. 5, the first and second analog integrators 2a, 2b operating in the z-domain, operation in the z-domain being indicative that the conversion means of FIG. 5 is discrete time in nature.

Section 2 of the Office Action attempts to traverse this argument on the basis that the z-domain is simply a transfer function for a sigma-delta converter. It is further asserted that the Sakimura application does not disclose a link between the z-domain and discrete-time operation. The Office Action also points to FIG. 3 of the Sakimura application as clearly disclosing a continuous conversion signal of a sigma-delta A/D converter with respect to time.

Whilst the above observations are noted, the following technical arguments should be borne in mind. Firstly, it is well understood in the art that use of the z-domain relates to discrete-time operation. If the Sakimura application wanted to make specific reference to continuous time operation, then reference would have been made to the s-domain. Clearly, the Sakimura application does explicitly refer to the z-domain, but not the s-domain and, in conjunction with common general knowledge in the technical field, it is submitted that reference to the z-domain unambiguously teaches discrete-time operation. If such an understanding of the state of the art is cannot be accepted, it is respectfully requested that counter-evidence be provided to support an assertion that reference to the z-domain, in relation to sigma-delta converters, does not teach discrete-time operation. With regard to the reference in the Office Action to FIG. 3 of the Sakimura application, it is submitted that FIG. 3 does, in fact, teach discrete-time operation. In this respect, it is assumed that a conclusion of continuous-time operation has been reached from a visual inspection of the apparent continuous nature of the waveforms shown. However, as would be appreciated by the skilled person, the level of magnification is not sufficiently great to show the true nature of the waveforms. It is therefore submitted that if one were to observe the waveforms of FIG. 3 at a greater level of magnification, one would see that the relevant signals are, in fact, discrete-time signals. Furthermore, as evidenced by the first 4 lines of paragraph [0096] and paragraph [0137], page 11, lines 4-7, the sigma-delta converters described in the Sakimura application are implemented using switched capacitor circuits. In this respect, it is very clear that use of switched capacitor circuits operate in a discrete-time mode. Therefore, the Sakimura application discloses a discrete time sigma delta modulator, which is not the same as the continuous time sigma delta converter.

In view of the reasoning provided above, Applicants submit that the Sakimura application does not anticipate Claim 1.

Claims 2 and 5-8 depend from Claim 1. By virtue of this dependence, Claims 2 and 5-8 are also novel over the Sakimura application.

Claim 4 provides for a method of compensating for known non-ideal characteristics in a continuous time sigma delta converter. As explained above in support of Claim 1, the

Sakimura application does not disclose a continuous time sigma delta converter. Accordingly, the Sakimura patent does not anticipate Claim 4.

Claims 15-18 depend from Claim 1. By virtue of this dependence, Claims 15-18 are also novel over the Sakimura application.

Claims 1, 4, 8, 17 and 18 are rejected under 35 USC §102(b) as being anticipated by US Patent No. 6,407,685 (hereinafter referred to as "the Händel patent"). Applicants are traversing this rejection.

As set out above, the application contains two independent claims, namely claims 1 and 4. Below, Applicants explain that the Händel patent does not disclose all of the elements of Claims 1 and 4.

The Händel patent discloses a Nyquist rate ADC, as indicated in the Office Action, in col. 5 of the Händel patent. FIG. 4A of the Händel patent shows an exemplary ADC and an associated calibrator (col. 8, lines 11-13). FIG. 4B shows exemplary details of an embodiment of calibration logic (col. 8, lines 35-37), and FIG. 4C shows another exemplary embodiment of calibration logic for the ADC (col. 9, lines 31-33).

Col. 5, line 25 simply explains that the ADC 105 converts a time-continuous and amplitude-continuous signal to a time-discrete and amplitude-discrete signal. This is true of all ADCs (as well as sigma-delta converters irrespective of whether they are continuous-time or discrete-time in nature). Likewise, col. 5, lines 35-38 simply explain that the ADC quantizes each sampled analog input signal into one of finite number of levels and represents each level a bit pattern. Col. 5, lines 42-48 simply explain that the principles of the invention disclosed in the Händel patent are applicable to other ADC environments, namely a sigma-delta ADC.

However, FIGS. 4A, 4B and 4C, and the above cited passages from col. 5 of the Händel patent, do not teach a "continuous time sigma-delta converter" as recited in claim 1. In this respect, col. 5, lines 42-48 are completely silent as to the nature of the sigma-delta converter. Indeed, col. 5, lines 42-48 simply explain that the principles of the invention of the Händel patent, namely the provision of the calibrator, can be employed in a sigma-delta ADC. Hence, the Händel patent does not actually disclose a sigma-delta ADC possessing the features recited in Claim 1, only that a particular inventive principle, namely calibration, can be applied to sigma-delta ADCs. This statement is made, in passing, in the Händel patent and is very ambiguous. The passages relied upon in Section 5 of the Office Action relate to FIGs. 4A, 4B and 4C of the Händel patent. In this respect, the ADCs employed in FIGs. 4A, 4B and 4C are Nyquist rate ADCs. Nyquist rate ADCs are very different to sigma-delta converters, because sigma-delta converters employ over-sampling, i.e. rates far greater than

the Nyquist rate. Additionally, a sigma-delta converter comprises a very different architecture to that of a Nyquist rate ADC, which possess sample and hold circuitry. Continuous time sigma-delta converters, in contrast, do not employ sample and hold circuitry in order to achieve the continuous nature of the mode of operation. Consequently, the Händel patent only relates to discrete-time circuits, and in particular with reference to FIGs. 4A, 4B and 4C, addresses non-linearities of Nyquist rate ADCs, which are, of course, discrete-time circuits. It should be pointed out that the nature of the input signal and the output signal in terms of whether or not they are continuous-time or discrete-time is not relevant in assessing whether a circuit itself is a continuous-time or discrete-time sigma-delta converter.

In view of the reasoning provided above, Applicants submit that the Händel patent does not anticipate Claim 1.

Claim 8 depends from Claim 1. By virtue of this dependence, Claim 8 is also novel over the Händel patent.

Claim 4 provides a method of compensating for known non-ideal characteristics in a continuous time sigma delta converted. As explained above in support of Claim 1, the Händel patent does not disclose a method of compensating for known non-ideal characteristics in a sigma delta converter, but particularly, a method of compensating for known non-ideal characteristics in a continuous time sigma delta converter as recited in Claim 4. Accordingly, the Händel patent does not anticipate Claim 4.

Claims 17 and 18 depend from Claim 1. By virtue of this dependence, Claims 17 and 18 are also novel over the Händel patent.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

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